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abrication and characterisation of U groove ›wer MOSFET

B Majumdar
Department of Electrical Engineering, Jadavpur University, Calcutta-700 032, India

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Abstract : Discrete MOSFETs with a modified truncated V-groove gate structure (in the shape of a 'U') has been fabricated on *p*-type Si. This structure has been fabricated by conventional IC technology processes using four masks only. The measured *I–V* characteristics of the fabricated devices shows some deviations from the ideal MOSFET due to unintentional presence of parasitic components because of the specific geometry of the device. To account for these deviations, a simple equivalent circuit is developed incorporating parasitic resistance components to explain the observed *I–V* characteristics and it is modelled with the circuit simulator SPICE.

Keywords : Power MOSFET, V-groove, parasitic components

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Introduction

gh current handling capability, good speed of operation and relatively high breakdown ltage are some of the essential requirements for MOSFETs being used as switching nents in a power circuit. Unfortunately, short channel MOSFETs have good current dling capability but they suffers from relatively low punch-through voltage. However, MOSFETs with gate structure in the form of a U groove, (*e.g.* UMOS) [1,2], it has found that the punch-through voltage is comparatively high, since the barrier ering phenomena and other hot-electron effects are suppressed due to the presence of groove corner [2,3]. The on-resistance of these devices are also low due to the absence : *n*–drift region. Moreover, it has been reported recently [4–7] that Power MOSFETs trench gate structure, have very low on-resistance as compared to other common ires.

In this paper, the fabrication of a 12 μm channel length and 110 μm channel width cated V-groove MOSFET (*i.e.* U-grooved gate structure) has been presented. The

electrical characteristics of the fabricated device and its associated electrical parameters including the equivalent circuit modelling has been discussed.

2. Fabrication

The cross-sectional view of a truncated V-groove lateral MOSFET using a four mask process is shown in Figure 1. Here, we have considered a *p*-type (100) Si (for *n*-channel devices) substrate having resistivity of 4.5 Ω. cm as our starting wafer. However, the processing steps for a *p*-channel device are same provided the starting wafer must be *n*-type Si with (100) orientation. Thick thermal oxide (5000 Å) is grown on the *p*-type chemically cleaned (100) Si wafer. Windows are opened to define the active device areas of length 200 μm and breadth 110 μm, using the first mask. A masked phosphorous diffusion (using liquid $POCl_3$ source maintained at 10°C) is performed through these windows in a controlled three-zone diffusion furnace for 2 hours predeposition and 15 mins drive-in at 1100°C for having a junction depth of approximately 3 μm. Using the second mask, a rectangular window is opened on n^+ diffused layer through which anisotropic etching of Si is performed. The anisotropic etchant used here is 80% hydrazine hydrate maintained at a temperature of 110°C [8]. The etching time has been so chosen that the V-groove etching is not complete. This type of etching will result in a truncated V-groove or U-shaped structure. Further, the etching is so controlled that the junction depth is less than the depth of the groove as shown in Figure 1. Measurements with interference microscope reveals that the width of the groove is 8 μm at the bed. This truncated V-groove separates out the source and drain region of the MOSFET. The gate oxide of the device is grown thermally having a thickness of 1000 Å. Using a third mask, windows are opened over the source and drain region for contact holes. Aluminium is deposited over the masked oxide and then metallisation is patterned to define bond pads and gate metal formation. Finally, the sample is annealed at 425°C for 5 mins in N_2 ambient. Figure 2 shows the photographs of a typical truncated lateral V-grooved MOSFET which has been fabricated.

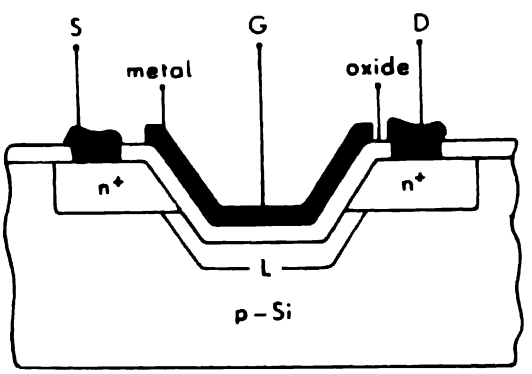

Figure 1. Cross sectional view of a lateral truncated V-Grooved MOSFET.

Plate 1

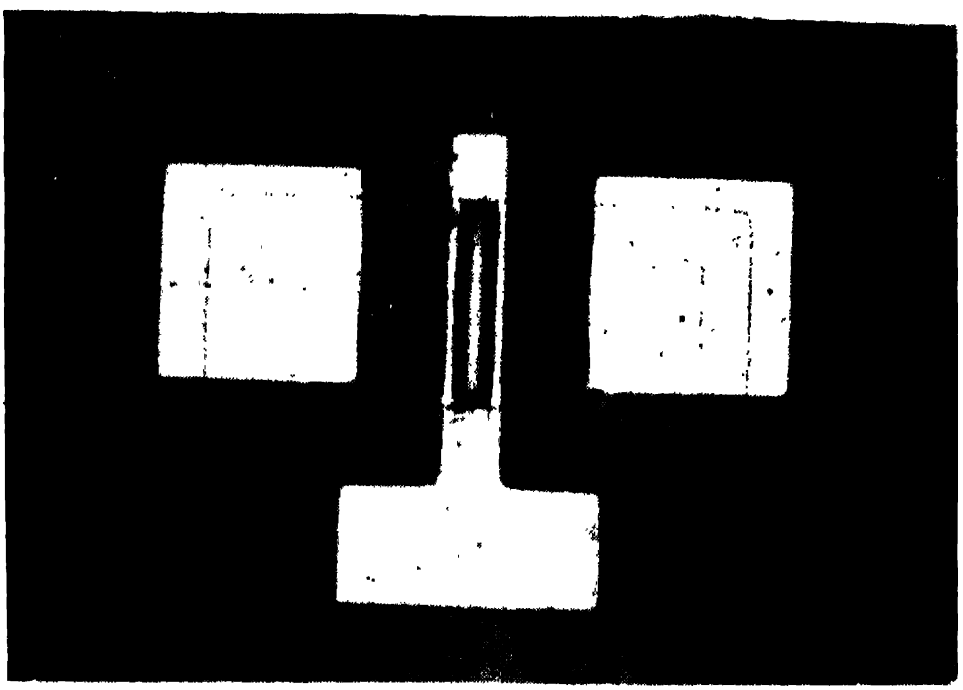

Figure 2. Photomicrograph of the top view of a truncated V-Grooved MOSFET.

3. Results and discussions

The fabricated MOSFET is characterised by measuring the d.c. *I-V* characteristics with substrate kept at ground potential as shown in Figure 3a. The specific on-resistance

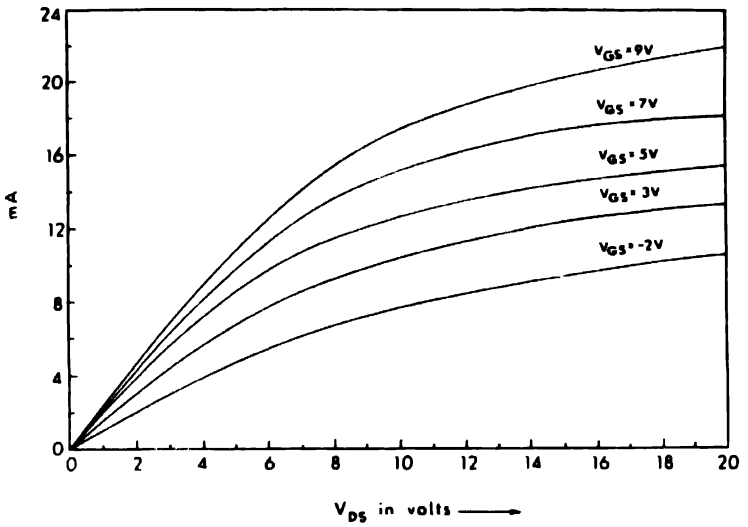

Figure 3(a). Measured dc I_D–V_{DS} characteristics of a truncated V-Groovred MOSFET.

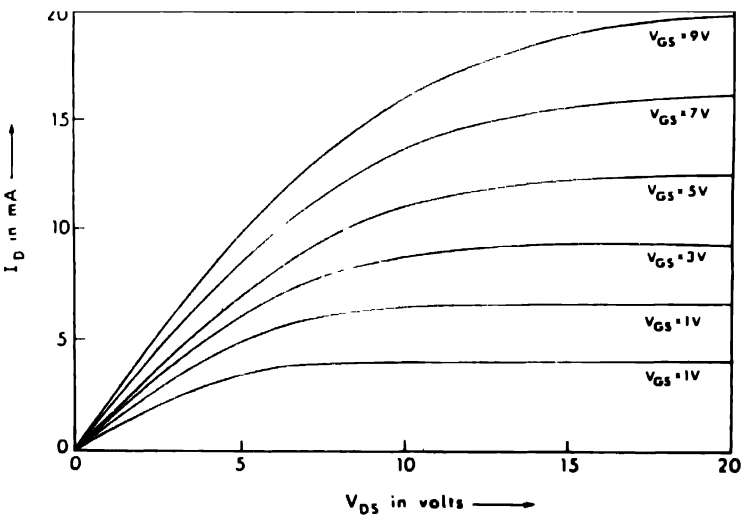

Figure 3(b). Ideal I_D–V_{DS} characteristics of a conventional MOSFET with planar gate having the same geometry and structure of the fabricated device.

estimated from the linear region of the characteristics, has been found to be 60 mohm. cm^2 at 9 V gate bias and it almost saturates beyond this gate bias. The specific on-resistance can be further reduced by reducing the channel length. The transconductance has been

found to be 1.5 mmho. at 6 V gate bias. The breakdown voltage of the fabricated devices ranges from 30 V-35 V. From the observed *I-V* characteristics, it is apparent that the observed *I-V* curves are found to deviate from the ideal characteristics as shown in Figure 3b. The measured *I-V* characteristics exhibits the following deviations from the ideal characteristics : (1) In the saturation region of the *I-V* characteristics, the drain current I_D increases almost linearly with V_{DS}, with a finite slope instead of being independent of V_{DS} for a particular V_{GS}. (2) The channel is more conducting even for negative gate bias voltage, thus reducing the threshold voltage to a negative value. This is perhaps due to the presence of high density of trapped charges at the SiO_2-Si interface [9], which can be removed by shallow Boron implant at the channel.

To model the above observed deviations of the *I-V* characteristics of the truncated V-groove MOSFETs from the ideal case, we have considered a ideal MOS structure represented by M1 in Figure 4. The MOS structure M1 has a planar gate configuration because of the simplicity of the structure in terms of mathematical modelling and also closeness of the structure to the fabricated device. An equivalent circuit shown in Figure 4 has been proposed incorporating parasitic components R_d, R_s and R_{sh}, to account for the observed characteristics.

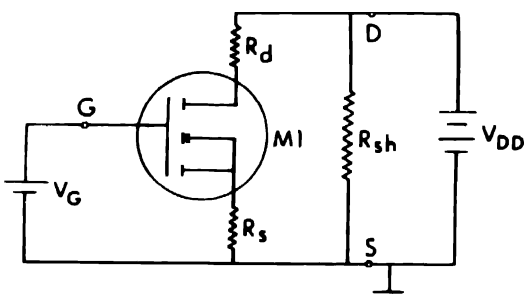

Figure 4. Equivalent circuit of the fabricated device including the parasitic resistance components

Using circuit simulator, SPICE [10], the above equivalent circuit has been solved and the simulated *I-V* results have been found to be in good agreement with the observed *I-V* measurements as shown in Figure 5. In the proposed model, shown in Figure 4, the ideal MOSFET M1 has been shown. In the MODEL card of M1, the channel-length modulation factor LAMBDA is negligible and resistances RD and RS of the SPICE model card have been the calculated values from RSH, and NRD and NRS parameters obtained from the device geometry and diffussion parameters. The shunt resistance RDS has been chosen to be zero. The model level has been restricted to LEVEL = 2, since we are mainly concerned with long channel devices. The gate oxide thickness is 1000 Å and the effective electron mobility of the channel is 350 cm^2/V-sec. The other parameters in the MODEL card has been incorporated directly from the device and material parameters of Si of the

fabricated device. Among the other device card parameters, the channel length (L) and the width (W), of the fabricated devices has been included.

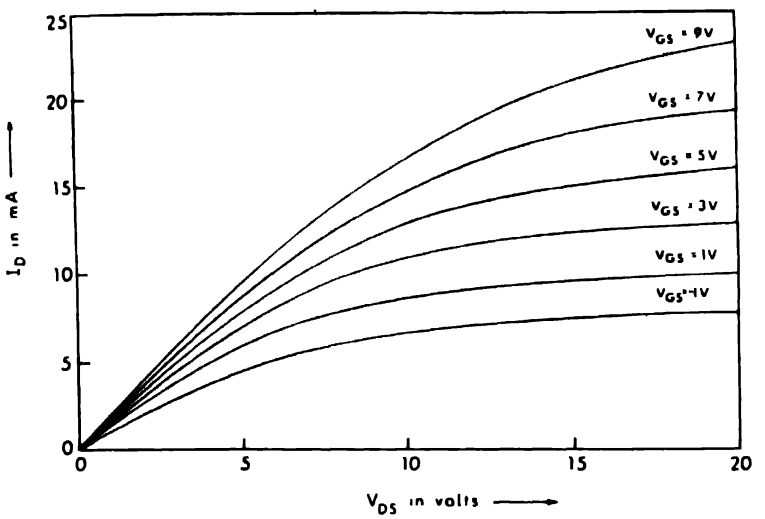

Figure 5. SPICE simulated d.c. I_D–V_{DS} characteristics of the equivalent circuit

It is well known that the MOS transistor channel is associated with two series parasitic resistances, one associated with the source and the other with the drain. Each of this resistance is composed of three components : (a) the resistance of the main body of the n^+ region, (b) the resistance of the metal contact to the n^+ region and (c) the resistance associated with the crowding of the current flow lines as the carriers move from the n^+ region to the thin inversion region. The contribution from the first component has been already incorporated in the SPICE model of MOSFET (RS and RD). The contributions from the other two components has been incorporated in the equivalent circuit of Figure 4 as R_s and R_d in the form of two effective parasitic resistances. The presence of high contact resistance (included in R_s and R_d) is due to the larger areas of the contact holes for the source and the drain. However, it is very difficult to calculate accurately the resistance due to the crowding effect for this specific structure of the device, which is only possible with a 3-D general purpose device simulator. But the experimental observations reveals the presence of R_s and R_d within the intrinsic device model. The effective shunt resistance R_{sh}, between the actual source and drain terminal in the equivalent circuit accounts for the linear increase of the drain current with the drain to source voltage in the saturation region. Hence, from the experimental observation, the values of R_s, R_d and R_{sh} (40 Ω, 40 Ω and 4 KΩ respectively) are selected to model the observed characteristics. So, in general, the I-V equation of the MOSFET with parasitic components can be written as [12]

$$I_D = \frac{\mu_{no} C_{ox}}{1+\theta(V_{GS}-V_T)} \frac{W}{L} \left\{ (V_{GS}-V_T)(V_{DS}-I_D R_p) - \frac{(V_{DS}-I_D R_p)^2}{2} \right\} + G_p (V_{DS}-I_D R_p), \quad (1)$$

where μ_{no} is the low field electron mobility in the channel, C_{ox} is the gate oxide capacitance per unit area, θ is the mobility degradation factor, V_T is the threshold voltage, R_p is the total series parasitic resistance and G_p is the substrate conductance to account for the parasitic substrate current.

Due to impact ionization, the channel electrons create electron hole pairs in the drain depletion region and some of the resulting holes then flow to the substrate creating a substrate current. This voltage dependent substrate current is then given by

$$I_{Sub} = (A_I/B_I)\left(V_{DS} - V_{Dsat}\right) e^{-B_I (V_D - V_{Dsat})/A_I}, \tag{2}$$

where A_I and B_I are related to the impact ionization coefficient α and electric field E as $\alpha = A_I e^{-B_I/E}$ and it plays an important role in determining the output characteristics of a MOSFET [11]. The above equation can be further simplified as

$$I_{Sub} = A_0 + A_1 V_{DS} + A_2 V_{GS} + A_3 V_{DS}^2 + A_4 V_{DS} V_{GS} + A_5 V_{GS}^2 + \cdots, \tag{3}$$

where A_0, A_1 *etc*. are constants for a specific device. This above phenomena is responsible for the incorporation of a finite shunt resistance in the model. We find from Figure 5 that in our case a voltage independent shunt resistance R_{sh} is the predominant factor. The output characteristics can be modelled accurately by introducing voltage dependent non-linear resistances. However, other factors such as edge effects at the gate terminals as well as effects from the U-groove corners will also become important to explain the output characteristics in addition to the above mentioned resistances.

The breakdown voltage of a U-grooved MOS is expected to be higher than a standard MOSFET, since the punch-through voltage which is given as [2]

$$V_{PT} = \frac{qN_A}{2\varepsilon_S}\left\{(r_j + L)^2\left[\ln\frac{(r_j + L)}{r_j} - \frac{1}{2}\right] + \frac{r_j}{2}\right\} - \phi_B \tag{4}$$

is improved due the lower value of the junction radius of curvature (r_j). In the above expression, L is the effective channel length and ϕ_B is the barrier height. For the present case, the measured breakdown voltage is not very large, but can be improved by better control of groove oxide thickness and other related parameters.

4. Conclusions

Lateral MOSFETs with modified truncated V-groove in the form of 'U' structured gate, has been fabricated using four masks only. The processing steps are simple and can be integrated with other components in an integrated circuit. The measurements of the different electrical parameters indicate that these transistors will perform well as Power MOSFETs in low voltage applications. The breakdown voltage of the device is expected to be larger than conventional MOSFET structures due to the presence of the groove corners. There is further scope of improvement of the breakdown voltage by better control of the gate oxide thickness at the termination points of the two different oriented surfaces and also

by removing the undulations present at the walls of the groove through controlled etching. The SPICE modelling shows that some unwanted parasitic components are active in determining some of the electrical parameters.

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References

[1] C A T Salama *Solid State Electron* **20** 1003 (1977)

[2] D A Smith and C A T Salama *Solid State Electron.* **23** 687 (1980)

[3] Shin ichiro Kimura, J Tanaka, H Noda, T Toyabe and S Ihira *IEEE Trans. on Electron Devices* **42** 94 (1995)

[4] T Syau, P Venkatraman and B J Baliga *IEEE Trans on Electron Devices* **41** 800 (1994)

[5] B J Baliga *IEEE Trans on Electron Devices* **ED-38** 1368 (1991)

[6] S C Sun and J D Plummer *IEEE Trans on Electron Devices* **ED-27** 356 (1986)

[7] Taylor Efland *Texas Instruments Tech. J.* **11** 10 (1994)

[8] D B Lee *J. Appl. Phys* **28** 4569 (1969)

[9] I Stoev and M Matev *Solid State Electron* **25** 987 (1982)

[10] Walter Banzhaf *SPICE Manual* (Englewood Cliffs, New Jersey : Prentice Hall) (1989)

T Y Chen, P K Ko and C Hu *IEEE Electron Device Lett.* **EDL-5** 505 (1984)

M J Deen and Z P Zuo *IEEE Trans on Electron Devices* **38** 1815 (1991)